

## ABSTRACT

A programmable logic device (PLD) includes a plurality of logic array blocks (LAB's) connected by a PLD routing architecture. At least one LAB includes a logic element (LE) configurable to arithmetically combine a plurality of binary input signals in a plurality of stages. The LE comprises look-up table (LUT) logic having K inputs (a "K-LUT"). The K-LUT is configured to input the binary input signals at respective inputs of the K-LUT logic cell and to provide, at a plurality of outputs of the K-LUT logic cell, respective binary result signals indicative of at least two of the plurality of stages of the arithmetic combination of binary input signals. An input line network includes a network of input lines, the input lines configurable to receive input signals from the PLD routing architecture that represent the binary input signals and to provide the input signals to the K-LUT. An output line network includes a network of output lines, the output lines configured to receive, from the K-LUT, output signals that represent the binary result signals and to provide the output signals to the PLD routing architecture. The described LUT's can perform arithmetic efficiently, as well as non-arithmetic functions.